Digital Phase Locked Loop Design And Layout | 0c875197601555539439e21fdd864e3b


Noise-Shaping All-Digital Phase-Locked Loops

Design, Simulation, Layout, and Test of a Digital Phase-locked Loop Circuit Design and Fabrication of a Controller for a Digital Phase Locked Loop Phase Locked Loop frequency synthesis is a key component of all wireless systems. This is a complete toolkit for PLL synthesizer design, with MathCAD, SIMetrix files included on CD, allowing readers to perform sophisticated calculation and simulation exercises. Describes how to calculate PLL performance by using standard mathematical or circuit analysis programs

Monolithic Phase-Locked Loops and Clock Recovery Circuits

Digital Phase-locked Loop Design Using SN54/74LS297 Abstract: In this thesis a
Full Digital Phase Locked Loop is designed and implemented in 0.13um technology node from TSMC. This full digital PLL is more advantageous than a traditional analog PLL because it eliminates the need for very fine analog voltage generated in a charge pump and it can be process independent. The focus of this thesis is to design and analyze a Digital Phase Locked Loop. This PLL has a lock range of 108MHz to 770MHz. A seven stage numerically controlled oscillator is implemented. Each inverter in the ring oscillator is driven by 21 tri-state inverters in parallel. To enable frequency control a 7 bit control word is decoded to enable these tri-state inverters. A second order integrating filter is used to average phase error and is clocked by control signals generated by a modified Phase Frequency Detector. This Full Digital PLL consumes 2.76mW of power when locked on at 720MHz.

Design of a Digital Phase-Locked Loop Filling the gap in the market dedicated to PLL structures for power systems Internationally recognized expert Dr. Masoud Karimi-Ghartemani brings over twenty years of experience working with PLL structures to Enhanced Phase-Locked Loop Structures for Power and Energy Applications, the only book on the market specifically dedicated to PLL architectures as they apply to power engineering. As technology has grown and spread to new devices, PLL has increased in significance for power systems and the devices that connect with the power grid. This book discusses the PLL structures that are directly applicable to power systems using simple language, making it easily digestible for a wide audience of engineers, technicians, and graduate students. Enhanced phase-locked loop (EPLL) has become the most widely utilized architecture over the past decade, and many books lack explanation of the structural differences between PLL and EPLL. This book discusses those differences and also provides detailed instructions on using EPLL for both single-phase applications and three-phase applications. The book’s major topics include: A basic look at PLL and its standard structure A full explanation of EPLL EPLL extensions and modifications Digital implementation of EPLL Extensions of EPLL to three-phase structures Dr. Karimi-Ghartemani provides basic analysis that helps readers understand each of the structures presented without requiring complicated mathematical proofs. His book is filled with illustrated examples and simulations that connect theory to the real world, making Enhanced Phase-Locked Loop Structures for Power and Energy Applications an ideal reference for anyone working with inverters, rectifiers, and related technologies.

Digital Phase-locked Loop Design Using SN54/74LS297

Phase-Locked Loop Synthesizer Simulation Unique book/disk set that makes PLL circuit design easier than ever. Table of Contents: PLL Fundamentals; Classification of PLL Types; The Linear PLL (LPLL); The Classical Digital PLL (DPLL); The All-Digital PLL (ADPLL); The Software PLL (SPLL); State Of The Art of Commercial PLL Integrated Circuits; Appendices; Index. Includes a 5 1/4" disk. 100 illustrations.

Fundamentals of Digital Logic with VHDL Design

Digital Phase-locked Loop Design for Naval Applications Phase Locked Loops (PLLs) are electronic circuits used for frequency control. Anything using radio
waves, from simple radios and cell phones to sophisticated military communications gear uses PLLs. The communications industry’s big move into wireless in the past two years has made this mature topic red hot again. The fifth edition of this classic circuit reference comes complete with extremely valuable PLL design software written by Dr. Best. The software alone is worth many times the price of the book. The new edition also includes new chapters on frequency synthesis, CAD for PLLs, mixed-signal PLLs, and a completely new collection of sample communications applications.

Design and Implementation of a Digital Phase-locked Loop A controller for an all digital phase locked loop which operates by pulse addition and removal is investigated. Being a first order system, the digital phase locked loop is more limited in regard to parameter controls than its second order analog counterpart. A loop with a fast lock time generally has poor phase/frequency accuracy, while a loop programmed for high accuracy will have slow lock time. Given that the digital phase locked loop is digitally programmable, a set of parameters may be selected which will minimize the lock time of the loop. Once the loop is locked, the parameters may be changed to alter the loop bandwidth and increase the loop accuracy. A controller circuit has been designed to adjust loop parameters in such a manner thereby optimizing loop performance. The exclusive-OR phase detector which is commonly used with the pulse addition/removal type digital phase locked loop has a phase lock range of plus or minus a quarter of a cycle. This work investigates the loop response to an incoming signal which is outside of the phase lock range of phase detector and inside the frequency lock range of the loop. A sub-circuit is proposed to improve the lock time of the loop when it encounters an incoming signal with these characteristics. The proposed circuits were designed using integrated circuit layout tools and submitted to a semiconductor manufacturer for fabrication. The controller concept and results of simulations and prototype experiments are presented.

Design of CMOS Phase-Locked Loops Most digital control architectures for power system applications require synchronization with the distribution system voltage. Therefore, a phase-locked loop (PLL), implemented in a DSP, is generally among the digital control blocks of the control system. The PLL analyzes the bus voltage and provides power system information for some of the other blocks to do further calculation. Thus, the performance of the PLL has a broad impact on the system performance. Small-scale power systems, such as naval systems, pose a challenging environment for PLL design due to voltage distortion and variation in the fundamental frequency that is large as compared to large terrestrial systems. Our objective is to improve the accuracy of the PLL digital block and hence enhance the digital control system. This research compares two PLL algorithms, as well as the use of a PI controller or lag controller with respect to their steady state and transient performance.

Design of 25MHz Digital Phase Locked Loop

Frequency Acquisition Techniques for Phase Locked Loops Fundamentals of Digital Logic With VHDL Design teaches the basic design techniques for logic circuits. It emphasizes the synthesis of circuits and explains how circuits are implemented in real chips. Fundamental concepts are illustrated by using small
examples, which are easy to understand. Then, a modular approach is used to show how larger circuits are designed. VHDL is used to demonstrate how the basic building blocks and larger systems are defined in a hardware description language, producing designs that can be implemented with modern CAD tools. The book emphasizes the concepts that should be covered in an introductory course on logic design, focusing on: Logic functions, gates, and rules of Boolean algebra
Circuit synthesis and optimization techniques
Number representation and arithmetic circuits
Combinational-circuit building blocks, such as multiplexers, decoders, encoders, and code converters
Sequential-circuit building blocks, such as flip-flops, registers, and counters
Design of synchronous sequential circuits
Use of the basic building blocks in designing larger systems
It also includes chapters that deal with important, but more advanced topics: Design of asynchronous sequential circuits
Testing of logic circuits
For students who have had no exposure to basic electronics, but are interested in learning a few key concepts, there is a chapter that presents the most basic aspects of electronic implementation of digital circuits. Major changes in the second edition of the book include new examples to clarify the presentation of fundamental concepts over 50 new examples of solved problems provided at the end of chapters NAND and NOR gates now introduced in Chapter 2 more complete discussion of techniques for minimization of logic functions in Chapter 4 (including the tabular method) a new chapter explaining the CAD flow for synthesis of logic circuits
Altera's Quartus II CAD software provided on a CD-ROM three appendices that give tutorials on the use of Quartus II software

Design of a Digital Phase-Locked-Loop
CMOS Universal Array Phase-Locked Loops for Wireless Communications: Digital, Analog and Optical Implementations, Second Edition presents a complete tutorial of phase-locked loops from analog implementations to digital and optical designs. The text establishes a thorough foundation of continuous-time analysis techniques and maintains a consistent notation as discrete-time and non-uniform sampling are presented. New to this edition is a complete treatment of charge pumps and the complementary sequential phase detector. Another important change is the increased use of MATLAB®, implemented to provide more familiar graphics and reader-derived phase-locked loop simulation. Frequency synthesizers and digital divider analysis/techniques have been added to this second edition. Perhaps most distinctive is the chapter on optical phase-locked loops that begins with sections discussing components such as lasers and photodetectors and finishing with homodyne and heterodyne loops. Starting with a historical overview, presenting analog, digital, and optical PLLs, discussing phase noise analysis, and including circuits/algorithms for data synchronization, this volume contains new techniques being used in this field. Highlights of the Second Edition: Development of phase-locked loops from analog to digital and optical, with consistent notation throughout; Expanded coverage of the loop filters used to design second and third order PLLs; Design examples on delay-locked loops used to synchronize circuits on CPUs and ASICS; New material on digital dividers that dominate a frequency synthesizer's noise floor. Techniques to analytically estimate the phase noise of a divider; Presentation of optical phase-locked loops with primers on the optical components and fundamentals of optical mixing; Section on automatic frequency control to provide frequency-locking of the lasers instead of phase-locking; Presentation of charge pumps, counters, and delay-locked loops. The Second
Edition includes the essential topics needed by wireless, optics, and the traditional phase-locked loop specialists to design circuits and software algorithms. All of the material has been updated throughout the book.

**Design and Testing of Digital Phase Locked Loop for High Speed Microprocessor Applications**

**Phaselock Techniques**

Phase-locked Loops A new and innovative paradigm for RF frequency synthesis and wireless transmitter design Learn the techniques for designing and implementing an all-digital RF frequency synthesizer. In contrast to traditional RF techniques, this innovative book sets forth digitally intensive design techniques that lead the way to the development of low-cost, low-power, and highly integrated circuits for RF functions in deep submicron CMOS processes. Furthermore, the authors demonstrate how the architecture enables readers to integrate an RF front-end with the digital back-end onto a single silicon die using standard ASIC design flow. Taking a bottom-up approach that progressively builds skills and knowledge, the book begins with an introduction to basic concepts of frequency synthesis and then guides the reader through an all-digital RF frequency synthesizer design: Chapter 2 presents a digitally controlled oscillator (DCO), which is the foundation of a novel architecture, and introduces a time-domain model used for analysis and VHDL simulation Chapter 3 adds a hierarchical layer of arithmetic abstraction to the DCO that makes it easier to operate algorithmically Chapter 4 builds a phase correction mechanism around the DCO such that the system's frequency drift or wander performance matches that of the stable external frequency reference Chapter 5 presents an application of the all-digital RF synthesizer Chapter 6 describes the behavioral modeling and simulation methodology used in design The final chapter presents the implementation of a full transmitter and experimental results. The novel ideas presented here have been implemented and proven in two high-volume, commercial single-chip radios developed at Texas Instruments: Bluetooth and GSM. While the focus of the book is on RF frequency synthesizer design, the techniques can be applied to the design of other digitally assisted analog circuits as well. This book is a must-read for students and engineers who want to learn a new paradigm for RF frequency synthesis and wireless transmitter design using digitally intensive design techniques.

**A Full Digital Phase Locked Loop**

Phase-Locked Loops for Wireless Communications This book presents a novel approach to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion. Readers will gain a deep understanding of ADPLLs and the central role played by noise-shaping. A range of ADPLL and TDC architectures are presented in unified manner. Analytical and simulation tools are discussed in detail. Matlab code is included that can be reused to design, simulate and analyze the ADPLL...
architectures that are presented in the book.

**Computer-aided Analysis and Design of a Digital Phase Locked Loop**

**Design of an All Digital Phase Locked Loop in FPGA**

Design of All Digital Phase-locked Loop in Serial Link Communication This volume introduces phase-locked loop applications and circuit design. Drawing theory and practice together, the book emphasizes electronics design tools and circuits, using specific design examples, addresses the practical details that lead to a working design. Wolaver assumes no specialized knowledge in the area covered, reviewing basics as necessary; makes heavy use of figures to support the understanding of phase-locked loop theory and circuit operation; extensively discusses frequency acquisition means, an intensely nonlinear phenomenon; treats injection locking, a practical and often confounding problem; and takes a unique approach to characterizing the phase-locked loop parameters.

**Synchronization in Digital Communication Systems**

Most digital control architectures for power system applications require synchronization with the distribution system voltage. Therefore, a phase-locked loop (PLL), implemented in a DSP, is generally among the digital control blocks of the control system. The PLL analyzes the bus voltage and provides power system information for some of the other blocks to do further calculation. Thus, the performance of the PLL has a broad impact on the system performance. Small-scale power systems, such as naval systems, pose a challenging environment for PLL design due to voltage distortion and variation in the fundamental frequency that is large as compared to large terrestrial systems. Our objective is to improve the accuracy of the PLL digital block and hence enhance the digital control system. This research compares two PLL algorithms, as well as the use of a PI controller or lag controller with respect to their steady state and transient performance.

**PLL Performance, Simulation and Design**

This book is intended for the reader who wishes to gain a solid understanding of Phase Locked Loop architectures and their applications. It provides a unique balance between both theoretical perspectives and practical design trade-offs. Engineers faced with real world design problems will find this book to be a valuable reference providing example implementations, the underlying equations that describe synthesizer behavior, and measured results that will improve confidence that the equations are a reliable predictor of system behavior. New material in the Fourth Edition includes partially integrated loop filter implementations, voltage controlled oscillators, and modulation using the PLL.

Phase-Locked Loops After a review of PLL essentials, this uniquely comprehensive workbench guide takes you step-by-step through operation principles, design procedures, phase noise analysis, layout considerations, and CMOS realizations for each PLL building block. You get full details on LC tank oscillators including modeling and optimization techniques, followed by design options for CMOS frequency dividers covering flip-flop implementation, the divider by 2 component, and other key factors. The book includes design alternatives for phase detectors that feature methods to minimize jitter caused by the dead zone effect. You also
find a sample design of a fully integrated PLL for WLAN applications that demonstrates every step and detail right down to the circuit schematics and layout diagrams. Supported by over 150 diagrams and photos, this one-stop toolkit helps you produce superior PLL designs faster, and deliver more effective solutions for low-cost integrated circuits in all RF applications.

Design and Implementation of an All Digital Phase Locked Loop Using a Pulse Output Direct Digital Frequency Synthesizer This modern, pedagogic textbook from leading author Behzad Razavi provides a comprehensive and rigorous introduction to CMOS PLL design, featuring intuitive presentation of theoretical concepts, extensive circuit simulations, over 200 worked examples, and 250 end-of-chapter problems. The perfect text for senior undergraduate and graduate students.

Design a Digital Phase-locked Loop (PLL) Circuit in FPGA

Special Phase/frequency Detector Design in Digital Phase Locked Loop for Multimode Transceiver

Phase-locked Loop Circuit Design Do you need to know how to develop more efficient digital communication systems? Based on the author's experience of over thirty years in industrial design, this practical guide provides detailed coverage of synchronization subsystems and their relationship with other system components. Readers will gain a comprehensive understanding of the techniques needed for the design, performance analysis and implementation of synchronization functions for a range of different modern communication technologies. Specific topics covered include frequency-looked loops in wireless receivers, optimal OFDM timing phase determination and implementation, and interpolation filter design and analysis in digital resamplers. Numerous implementation examples help readers to develop the necessary practical skills, and slides summarizing key concepts accompany the book online. This is an invaluable guide and essential reference for both practicing engineers and graduate students working in digital communications.

Design Methodology for RF CMOS Phase Locked Loops Featuring an extensive 40 page tutorial introduction, this carefully compiled anthology of 65 of the most important papers on phase-locked loops and clock recovery circuits brings you comprehensive coverage of the field—all in one self-contained volume. You'll gain an understanding of the analysis, design, simulation, and implementation of phase-locked loops and clock recovery circuits in CMOS and bipolar technologies along with valuable insights into the issues and trade-offs associated with phase locked systems for high speed, low power, and low noise.

Design of a Testable Jitter Free Digital Phase Locked Loop

DIGITAL PHASE-LOCKED LOOP DESIGN FOR NAVAL APPLICATIONS.

Design of a Digital Phase Locked Loop for Robust Symbol Synchronization in a DECT Receiver A digital phase-locked-loop circuit developed by The Charles Stark Draper Laboratory, Inc. and sponsored by the Air Force Avionics Laboratory, was successfully implemented on an RCA TCC 051 universal array (type number TCC
Twenty engineering prototypes were evaluated by the contracting agency and found acceptable. Additional 150 units were subsequently supplied. A market study was made of the commercial applicability of the DPLL LSI design.

Enhanced Phase-Locked Loop Structures for Power and Energy Applications

All-Digital Frequency Synthesizer in Deep-Submicron CMOS A greatly revised and expanded account of phaselocktechnology The Third Edition of this landmark book presents new developments in the field of phaselock loops, some of which have never been published until now. Established concepts are reviewed critically and recommendations are offered for improved formulations. The work reflects the author's own research and many years of hands-on experience with phaselock loops. Reflecting the myriad of phaselock loops that are now found in electronic devices such as televisions, computers, radios, and cellphones, the book offers readers much new material, including: * Revised and expanded coverage of transfer functions * Two chapters on phase noise * Two chapters examining digital phaselock loops * A chapter on charge-pump phaselock loops * Expanded discussion of phase detectors and of oscillators * A chapter on anomalous phaselocking * A chapter on graphical aids, including Bode plots, root locus plots, and Nichols charts As in the previous editions, the focus of the book is on underlying principles, which remain valid despite technological advances. Extensive references guide readers to additional information to help them explore particular topics in greater depth. Phaselock Techniques, Third Edition is intended for practicing engineers, researchers, and graduate students. This critically acclaimed book has been thoroughly updated with new information and expanded for greater depth.

Design, Simulation, and Layout of a Monolithic Current-mode Digital Phase Locked Loop

Phase-Locked Loops for Wireless Communications

Clock Synthesizer Design with Analog and Digital Phase Locked Loop How to acquire the input frequency from an unlocked state A phase locked loop (PLL) by itself cannot become useful until it has acquired the applied signal's frequency. Often, a PLL will never reach frequency acquisition (capture) without explicit assistive circuits. Curiously, few books on PLLs treat the topic of frequency acquisition in any depth or detail. Frequency Acquisition Techniques for Phase Locked Loops offers a no-nonsense treatment that is equally useful for engineers, technicians, and managers. Since mathematical rigor for its own sake can degenerate into intellectual "rigor mortis," the author introduces readers to the basics and delivers useful information with clear language and minimal mathematics. With most of the approaches having been developed through years of experience, this completely practical guide explores methods for achieving the locked state in a variety of conditions as it examines: Performance limitations of phase/frequency detector-based phase locked loops The quadricorrelator method for both continuous and sampled modes Sawtooth ramp-and-sample phase detector and how its waveform contains frequency error information that can be extracted The benefits of a self-sweeping, self-extinguishing topology Sweep methods using
quadrature mixer-based lock detection. The use of digital implementations versus analog Frequency Acquisition Techniques for Phase Locked Loops is an important resource for RF/microwave engineers, in particular, circuit designers; practicing electronics engineers involved in frequency synthesis, phase-locked loops, carrier or clock recovery loops, radio-frequency integrated circuit design, and aerospace electronics; and managers wanting to understand the technology of phase-locked loops and frequency acquisition assistance techniques or jitter attenuating loops. Errata can be found by visiting the Book Support Site at: ahref="http://booksupport.wiley.com/"http://booksupport.wiley.com/a

Digital Phase Locked Loop Design For Communication System. This book is intended for the graduate or advanced undergraduate engineer. The primary motivation for writing the text was to present a complete tutorial of phase-locked loops with a consistent notation. As such, it can serve as a textbook in formal classroom instruction, or as a self-study guide for the practicing engineer. A former colleague, Kevin Kreitzer, had suggested that I write a text, with an emphasis on digital phase-locked loops. As modern designers, we were continually receiving requests from other engineers asking for a definitive reference on digital phase-locked loops. There are several good papers in the literature, but there was not a good textbook for either classroom or self-paced study. From my own experience in designing low phase noise synthesizers, I also knew that third-order analog loop design was omitted from most texts. With those requirements, the material in the text seemed to flow naturally. Chapter 1 is the early history of phase-locked loops. I believe that historical knowledge can provide insight to the development and progress of a field, and phase-locked loops are no exception. As discussed in Chapter 1, consumer electronics (color television) prompted a rapid growth in phase-locked loop theory and applications, much like the wireless communications growth today. xiv Preface Although all-analog phase-locked loops are becoming rare, the continuous time nature of analog loops allows a good introduction to phase-locked loop theory.